The University of Malta invites you to register for the online course **Comprehensive VHDL Design: VLSI Digital Design for FPGA** offered by the University Semiconductors Competence Centre.

Dates: 23-26 March 2026
Time: 09:00-16:00 each day (CET)
Location: Online Sessions

This four-day online course is taught in English and is available free of charge, but has a limited number of slots. It is designed for both beginners in digital design and experienced designers who want to learn VHDL for FPGA development. By the end of the course, participants will be able to write clear, synthesizable VHDL code and understand how it maps to hardware; verify functionality by creating self-checking testbenches to simulate and validate designs; and ensure quality by checking designs with industry-standard tools to catch errors early.

Day 1 (seminar): VHDL Fundamentals & Hierarchy - Introduction to VHDL structuring, declaration of Entities & Architecture, component Instantiation and the use of the Simulation software.

Day 2 (seminar): Synthesis, Finite State Machines & Parametrisation - Mapping of VHDL code to FPGA hardware, designing sequential circuits and implementing memory structures.

Days 3-4 (hands-on): These sessions allow delegates to develop various VHDL applications using Siemens Questa Simulation software.

For more details on the course and to register your attendance, visit:
https://www.um.edu.mt/uscc/upskillingcourses/comprehensivevhdldesigncourse/

If you have any questions or require additional information, feel free to reach out to us. We are looking forward to hearing from you.

Regards,
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